Journal of Power Sources 267 (2014) 622–628

Contents lists available at ScienceDirect

Journal of Power Sources

journal homepage: www.elsevier.com/locate/jpowsour

# A miniature fuel cell with monolithically fabricated Si electrodes – Reduction of residual porous Si on catalyst layer

Masahiro Kobayashi [a], Takahiro Suzuki [a], Masanori Hayase [a, b, *]

[a] Faculty of Science and Technology, Tokyo University of Science 2641 Yamazaki, Noda-shi, Chiba-ken, 278-8510, Japan
[b] Research Center for Green and Safety Sciences, Tokyo University of Science 1-3 Kagurazaka, Shinjuku, Tokyo, 162-8601, Japan

## HIGHLIGHTS

- Porous Pt layer was formed on a Si substrate using anodized porous Si.
- Miniature fuel cell was build using the porous Pt as a catalyst.
- Residual porous Si layer was observed on the porous Pt catalyst layer and could not be removed by additional etching.
- Process condition was optimized to reduce the residual porous Si.
- Highest power density of 450 mW $cm^{-2}$ comparable to large scale fuel cells was obtained by a cell having least residual porous Si.

## ARTICLE INFO

*Article history:*
Received 11 April 2014
Accepted 20 May 2014
Available online 4 June 2014

*Keywords:*
MEMS
Fuel cell
Porous silicon
Plasma etching
Anodization
Wet plating

## ABSTRACT

Higher performance was obtained in our miniature fuel cells by reducing the residual porous Si on catalyst layers. We have developed a miniature polymer electrolyte fuel cell by forming monolithic Si electrodes with MEMS techniques, in which a catalyst layer was synthesized on a Si chip by modifying porous Si to porous Pt by a wet plating process. As a result of technical limitations in the fabrication process, porous Si was left on the porous Pt catalyst layer. The residual porous Si was intended to lower the fuel cell performance by blocking reactant gas supply, and the effect of the residual porous Si on fuel cell performance was studied. The anodization conditions for porous Si formation were varied, and several prototype fuel cells were prepared with residual porous Si of different thickness. It was confirmed that a thick residual porous Si layer reduced cell performance, and high power density comparable to conventional large scale fuel cells was obtained with the least residual porous Si.



## 1. Introduction

Fuel cells have been developed for local energy supply to homes or vehicles, because high efficiency is expected even in such a small scale system and low temperature. Home use fuel cells are now available commercially, and fuel cell vehicles are about to go into mass production. Portable electronic devices now demand higher performance power sources. Presently, lithium ion batteries have met the demand for use in those small scale devices, and extensive studies about lithium ion batteries have been published. Miniature fuel cells are also attractive as power sources for these devices, especially for their high energy density and quick recharge potential. Some products, such as Toshiba Dynario™, had been also sold, but they did not achieve commercial success. Further miniaturization will be needed to meet commercial demand however.

Micro electromechanical systems (MEMS) fabrication technology is an important tool in miniaturizing fuel cell structure, and is well suited to mass production. Several miniature fuel cell prototypes have been reported using MEMS techniques [1–17] Most of them are of polymer electrolyte membrane (PEM) type, in which catalyst layers were put on both sides of the PEM. For example, Kelley et al. fabricated a direct methanol fuel cell (DFMC) with Si catalyst layer supporters, and demonstrated that the resulting miniaturized DMFC has almost the same performance as state-of-the-art fuel cells having conventional structure [1]. Novel electrolyte concepts have also been explored [13,14,16], and chemically modified porous Si shows promising results [16]. Most studies involve conventional catalyst layers, which consist of carbon black with catalyst metal particles. MEMS techniques are generally

* Corresponding author. Faculty of Science and Technology, Tokyo University of Science 2641 Yamazaki, Noda-shi, Chiba-ken, 278-8510, Japan. Tel./fax: +81 4 7122 1375.
*E-mail address:* mhayase@rs.noda.tus.ac.jp (M. Hayase).

http://dx.doi.org/10.1016/j.jpowsour.2014.05.108
0378-7753/

applied on monolithic structures, and treatment using powders such as carbon black is not appropriate. Kuriyama et al. have proposed a novel catalyst layer structure using carbon nanotubes grown on a Si chip, but the performance was not comparable to conventional powder based catalyst. Recently, miniaturization of a solid oxide fuel cell (SOFC) has been proposed by Prinz et al. [17]. A MEMS structure with thin film solid oxide electrolyte and catalyst layer was realized. High output was demonstrated, and several research groups are now studying the concept [17–20], although there are difficulties in high temperature treatment and catalyst durability.

We also have proposed a miniature polymer electrolyte fuel cell (PEFC) design, using monolithic Si based electrodes [21]. We recently found that a porous Pt layer can be obtained by immersing high-porosity porous Si into a Pt plating bath containing HF [22]. X-ray energy dispersive spectroscopy (EDS) analysis revealed that the porous layer consists mostly of Pt; little signal from Si was observed. Using the porous Pt layer as catalyst and an etch-stop layer, fuel channels were opened by dry etching on the Si electrodes. Two Si electrodes were combined with a PEM sheet and 230 μm thick prototype cells were constructed. A high output of 145 mW $cm^{-2}$ for MEMS based fuel cells was demonstrated by a prototype cell. High power density beyond conventional fuel cells is expected by stacking cells using the thin feature. But performance has still been poorer than conventional large scale fuel cells and varied from cell to cell. It was difficult to set up a practical reaction area, around 1 $cm^2$, while maintaining the power density. These difficulties must be solved.

It is often observed that porous Si remains on the hexagonal fuel channel bottoms, as shown in Fig. 1. We suppose that some porous Si is needed at the interface between the porous Pt and bulk crystalline Si in order to preserve the porous Pt layer on the chip. But we suspect that the residual porous Si on the fuel channel bottoms impairs cell performance by blocking fuel supply to the catalyst layer, and this might explain the performance instability. Higher output power may also be expected by eliminating the obstruction for the fuel supply. The porous Si layer is formed by anodization in a HF solution. Adjustment of the porous Si layer thickness on the μm scale is not easy, because the rate of formation of anodized porous Si layer is sensitive to the concentration of impurities [23], which varies even in an identical Si wafer lot, and we have not concentrated on precise control of the porous Si layer thickness. In this study, therefore, the fabrication process was optimized to reduce the residual porous Si, and the effect of the residual porous Si is discussed.

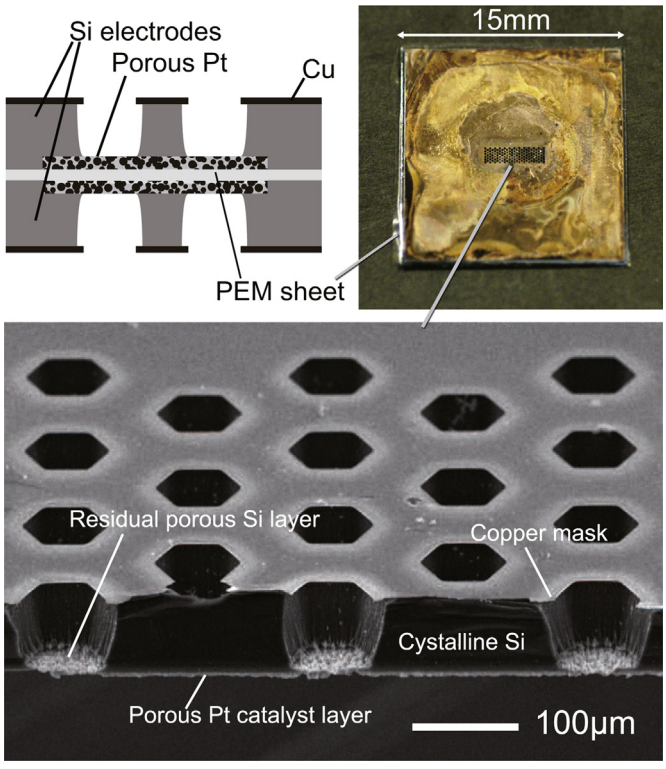


**Fig. 1.** Overview of our miniature fuel cell. Two monolithic Si electrode chips and a PEM sheet were combined. Lower SEM image is a perspective view of the cleaved Si electrode chip. Fuel channels were opened by RIE with copper mask. Rough products, which we call "residual porous Si layer", were frequently observed on channel bottoms. Simple hexagonal openings were used in this study. Fuel supply trenches will be formed on the Si chip and openings will be connected, and chip stack is planned.

## 2. Experimental

### 2.1. A miniature fuel cell

The fabrication process of the miniature fuel cells is detailed in previous reports [21,22]. Fig. 2 shows the fabrication procedure for the monolithic electrode. The porous Pt layer, which works as a catalyst layer, is formed on a Si wafer. After the porous Pt catalyst layer has formed, reactive ion etching (RIE) is applied and fuel channels are opened. A PEM sheet is hot-pressed with two Si electrodes, and production of a fuel cell is then completed. The Si wafer is about 110 μm thick, and the total thickness of a cell is about 230 μm. The experimental conditions of each process are as follows.

### 2.2. Catalyst layer formation

Formation of the catalyst layer involves two processes, namely anodization of crystalline Si and Pt plating. Apparatus and procedure identical to the previous study [21,22] were used in the formation of the catalyst layer. Table 1 shows the conditions for the process, which are determined by trial and error. All processes were performed in a refrigerated chamber. Single crystalline Si wafers were cut into 15 mm square chips by a blade dicing machine, and these chips were used as specimens. Porous Si was formed by anodization of a crystalline Si chip in a concentrated HF solution. Based on the previous work, we chose a current modulation in which the anodization current was reduced linearly from 60 to 0 mA $cm^{-2}$ over 1380 s. Although the thickness of the resulting porous Si layer was excessive with these conditions, they ensure the mechanical strength of the chip. In the present work, this current modulation was changed slightly. After the anodization, the porous Si layers were rinsed with acetone to prevent oxidation by water. Immediately after acetone rinsing, immersion plating was performed for 15 min.

### 2.3. Reactive ion etching

A conventional parallel plate reactive ion etching (RIE) system (Samco RIE-10N, Japan) was used, and 18 sccm of $SF_6$ and 4 sccm of $O_2$ gas were supplied for etching of the Si wafer. The back side of the porous Pt layer, in which the bulk Si layer remained, was etched, and channels for gas supply were formed. In the RIE process, a porous Pt layer is intended to act as a stopping layer of the etching, because the etching rate is low at the porous metal layer. To create gas supply channels to the catalyst layer, an array of holes was etched. RIE was interrupted a few times so that the specimen could be observed by optical microscope to verify that the bottoms reached the porous layer. The residual porous Si layer after the RIE process was observed by a scanning electron microscope (JEOL JCM-5100, Japan). Elemental analysis and high resolutional

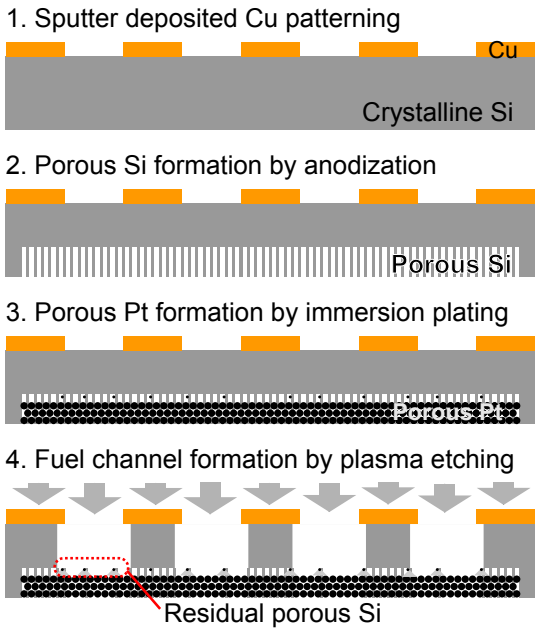


**Fig. 2.** Schematic view of the monolithic Si electrode fabrication procedure. 1. Sputter deposited copper film was pattened by conventional photolithography and wet etching. The copper film works as a mask for plasma etching and also as an electrical contact at anodization and power generation tests. 2. Porous Si is formed by anodization in a HF solution. The Si chip is placed in a fluorocarbon resin vessel and opposite side of copper film faces to the HF solution. 3. After anodization, the HF solution is replaced to the Pt plating solution, and the porous Pt layer is formed. 4. Plasma etching is applied on the copper film side, and fuel channel to the catalyst layer are made. Two electrode chips are combined with a PEM sheet and a prototype cell is made.

**Table 1**
Conditions for fabrication of the porous Pt layer.

| | | |
|---|---|---|
| Property of Si substrate | Crystal orientation | (100) |
| | Doping type | N (As doped) |
| | Resistivity | 0.001–0.003 Ω cm |
| Anodization | Composition of solution | Water:HF(46%):Ethanol = 5:3:2 (wt.) |
| Pt immersion plating | Composition of solution | 20 mM $H_2PtCl_6$ + 1 M $H_2SO_4$ + 450 mM HF |
| | Plating time | 15 min |
| | Temperature | 283 K |

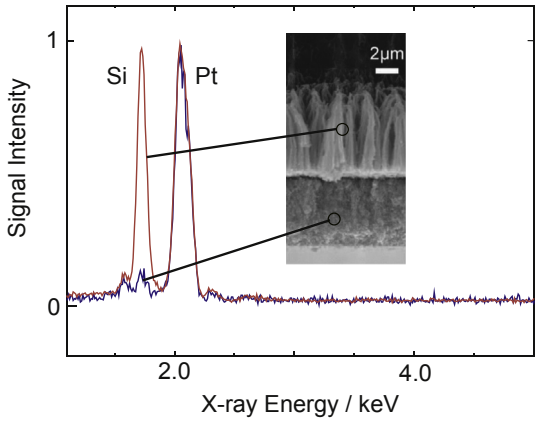


**Fig. 4.** Elemental analysis of the porous layers by EDS. A cross section of the cleaved chip was analyzed. The red line shows the spectrum at the residual porous Si layer, and the black line shows the spectrum at the porous Pt layer. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

observation were carried out by a further scanning electron microscope (Hitachi S-4200, Japan) equipped with an energy dispersive X-ray spectroscopy (EDS) system (EDAX, Mahwah, NJ).

### 2.4. Prototype assembly and power generation

Two Si electrodes were hot-pressed onto either side of a polymer electrolyte membrane (PEM) at 373 K and 0.09 MPa for 30 min, and a prototype cell was constructed. The fuel channel holes were patterned in a rectangle of side 1 mm × 4 mm. As the etching mask,

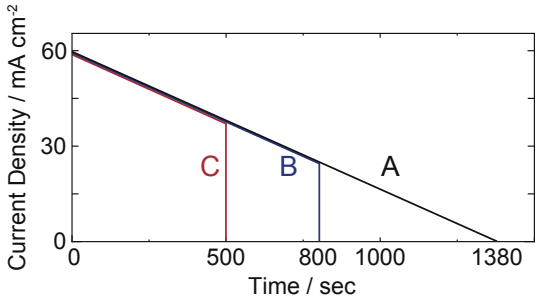


**Fig. 5.** Current density modulations used in the anodization of crystalline Si. (A) Was the conventional modulation determined by trial and error in the previous study. (B) and (C) Were tested to obtain less residual porous Si layer.

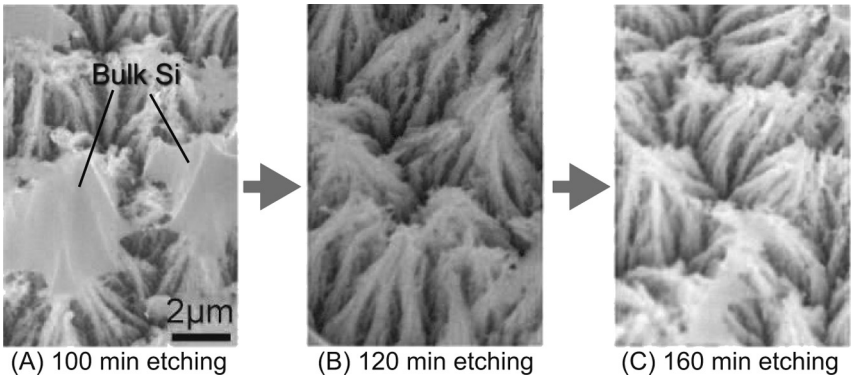


**Fig. 3.** Effect of additional etching on the residual porous Si layer. The residual layer on the channel bottoms was observed by SEM. (A) After 100 min etching, (B) after additional 20 min (total 120 min) etching, and (C) after a further 40 min (total 160 min) etching. All images were taken on the ame chip.

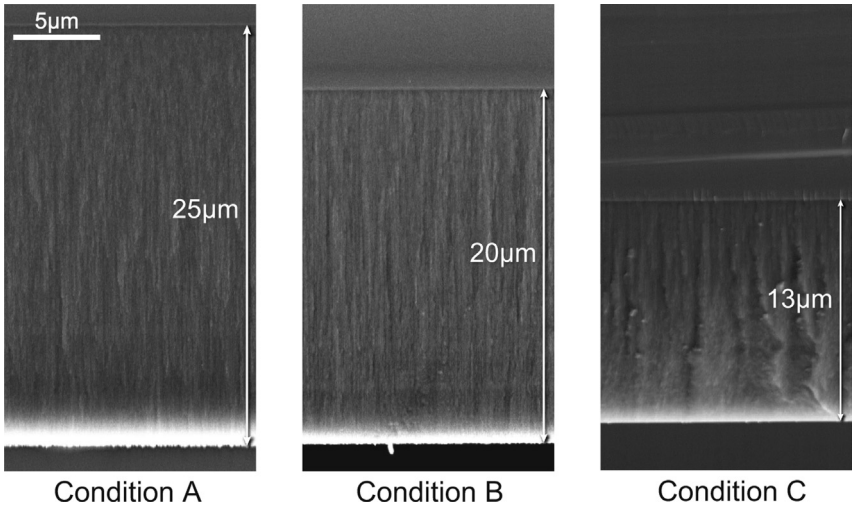


**Fig. 6.** Cross-sections of the porous Si layers obtained by three different anodization current modulations.

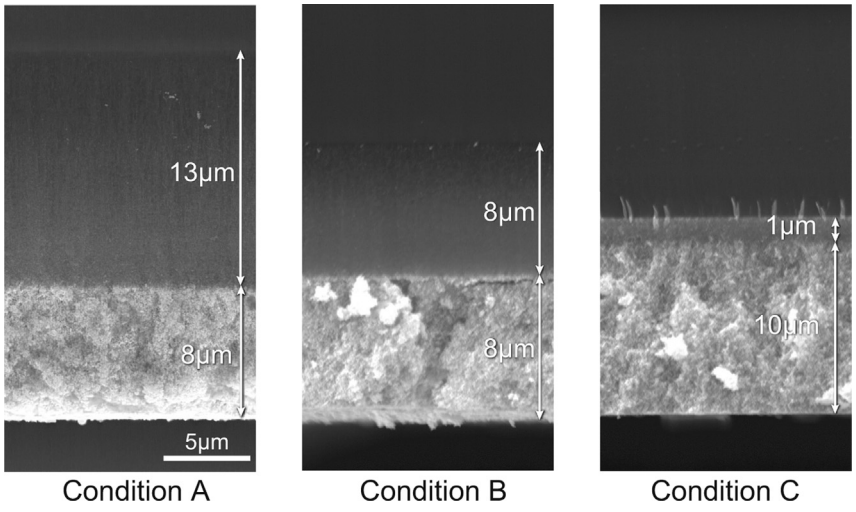


**Fig. 7.** Cross sections of the porous Pt layers after Pt immersion plating. An identical plating process was applied to the three porous Si layers of differeing thickness prepared by the three current modulations.

regular hexagonal openings of side length 100 μm were arrayed with 100 μm gap. The PEM used in the prototypes was a SF-150 (Toagosei Co. Ltd., Japan). The membrane is a pore-filling electrolyte membrane, and was used to protect the porous Pt layers from destruction by membrane swelling in humidified conditions. Nafion solution (DE520, Wako Chemicals) diluted by 1.7% with isopropyl alcohol was used as an adhesive in the assembly process.

The prototype cells were put in an aluminum casing, and 8 sccm of hydrogen gas and 4 sccm of oxygen gas were fed into the cells in a temperature-controllable chamber at 313 K. The hydrogen gas was humidified by bubbling through a water containing tank which was heated to the testing temperature. Oxygen was supplied as dry gas. The cell potential was scanned at 2 mV $s^{-1}$ using a potentiostat (Hokuto-Denko HABF5001, Japan) controlled by a computer running our own data acquisition software.

## 3. Results and disucssion

### 3.1. Effect of excess etching time on the residual porous Si layer

We know empirically that porous Si can be etched by RIE much more quickly than crystalline Si. The residual porous Si layer can therefore presumably be removed by expanding the etching time. Fig. 3 shows the bottom of the fuel channel after the RIE process. On the specimen Si chip, a porous Si layer about 20 μm thick was prepared by anodization, and a porous Pt layer about 10 μm thick was formed. Fig. 3(a) shows the channel bottom when the porous layer began to appear after 100 min of the RIE process. The etching depth was about 90 μm. Bulk crystalline Si islands were still observed. Fig. 3(b) & (c) show the bottom with 20 and 60 min additional etching after the porous layer appeared. Bulk Si islands were all etched away by the additional etching. In Fig. 3(b) & (c), however there were still porous or fiber bundle-like residual layers on the bottom. There were no obvious differences between Fig. 3(b) and (c). The residual layer had high resistivity to RIE, and it was difficult to remove the residual layer by further etching.

Fig. 4 shows EDS spectra of the porous layer. The spectra were normalized using Pt peaks. The residual porous Si region (red line) and porous Pt region (blue line) (in web version) were analyzed. Although a Pt deposit was scarcely observed on the residual porous Si region according to SEM observation, an obvious Pt signal was detected in the residual layer. In the porous Pt region it was reconfirmed that the Si signal is very small. Pt is deposited in the

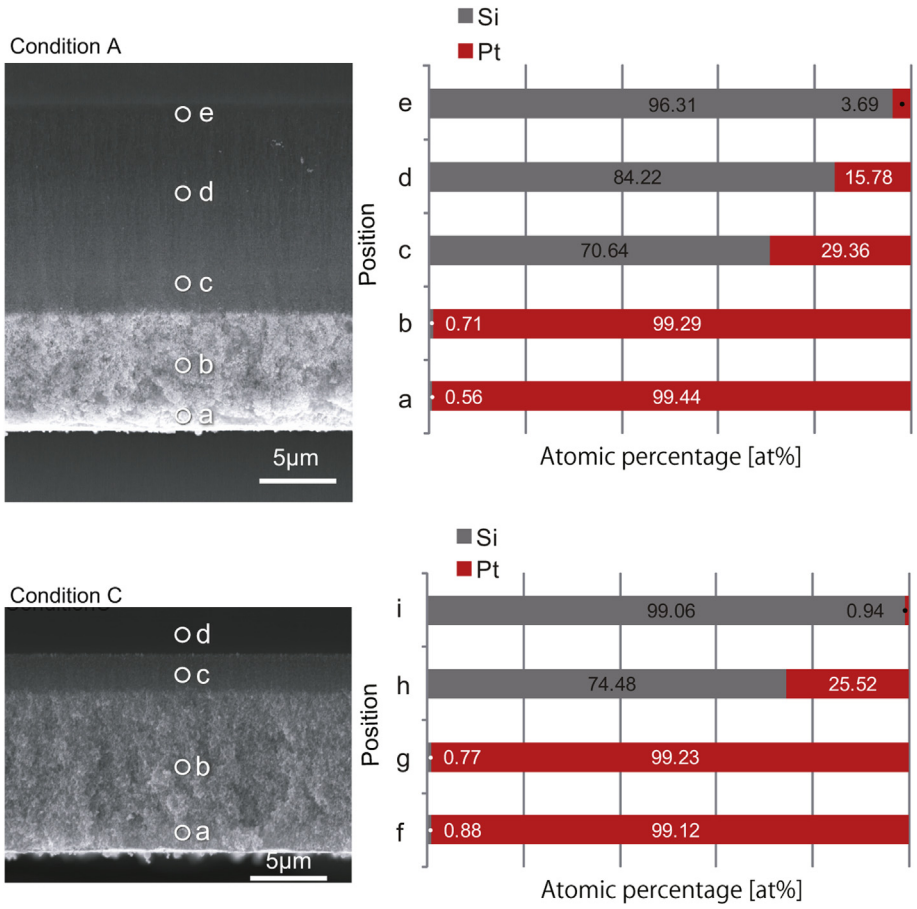


**Fig. 8.** EDS elemental analyses of several points on the cross-section of cleaved chips. Quantitative analysis mode of the EDAX accessory software was used with default setting, and two elements (Pt and Si) were quantified.

residual porous Si layer, and this Pt deposit causes the high resistivity of the residual layer to RIE.

### 3.2. Adjustment of porous Si layer thickness

Additional etching proved unable to remove the residual porous Si layer. The thickness of the porous Si layer was optimized to reduce the residual porous Si layer by adjusting the anodization current. The thickness of the porous Si layer is in general not proportional to the applied charge even if the constant current density was applied, because the concentration of hydrofluoric acid and other components at the pore tip changes as the porous layer grows. Moreovers, porous Si formation by anodization is sensitive to the doping concentration of the Si wafer. The anodization current was therefore determined empirically. To ensure adequate reproducibility in this work, the 15 mm square Si chips used in the experiments were cut from two wafers selected from the ten wafers.

Three anodization conditions (A–C) shown in Fig. 5 were tested. The applied charges in conditions A–C were respectively 41.4, 34.1, and 24.6C $cm^{-2}$. Cross-sectional SEM images after anodization are shown in Fig. 6. The thickness of the porous Si layer was reduced by shortening the anodization time. The resulting thicknesses of the porous Si layers under conditions A–C were 25, 20, and 13 μm respectively. As usual, the porous layer thickness was not proportional to the applied charge.

Immersion plating was performed on the chips prepared under the above conditions. Fig. 7 shows cross-sectional SEM images after the immersion plating. Almost no porous Si layer was observed on a chip prepared under condition C, but a thick porous Si layer remained in conditions A and B. EDS elemental analyses were performed at several points on the cross-section, and the results are shown in Fig. 8. The atomic percentages shown in the figures were estimated by the EDS accessory software (EDAX Genesis) with default setting, and were not calibrated values. It was found that Pt deposition had penetrated into the residual porous Si layer.

Finally, RIE was applied and the resulting through-chip porous catalyst area was observed. Fig. 9 shows cross-sections and inclined views of the channel bottoms. It was found that the residual porous Si layer was successfully reduced by shortening the anodization time. Almost no residual porous Si layer was observed with condition C, and there was no severe destruction of the porous Pt structure as shown in Figs. 9 and 10. Several micro-cracks were observed on the channel bottom, but they did not appear to penetrate deeply.

### 3.3. Cell performance

Three different thick residual porous Si layers were prepared, and the effect of the residual porous Si layer on the fuel cell performance was examined. More than three prototypes were prepared with three conditions A–C in order to examine the reproducibility of the cell fabrication process. Typical polarization curves are shown in Fig. 11. The current density was calculated assuming that the reaction area was $1 \times 4$ $mm^2$. It was found that cell performance was improved by reducing the residual porous Si layer, and highest performance was obtained in the cell with almost

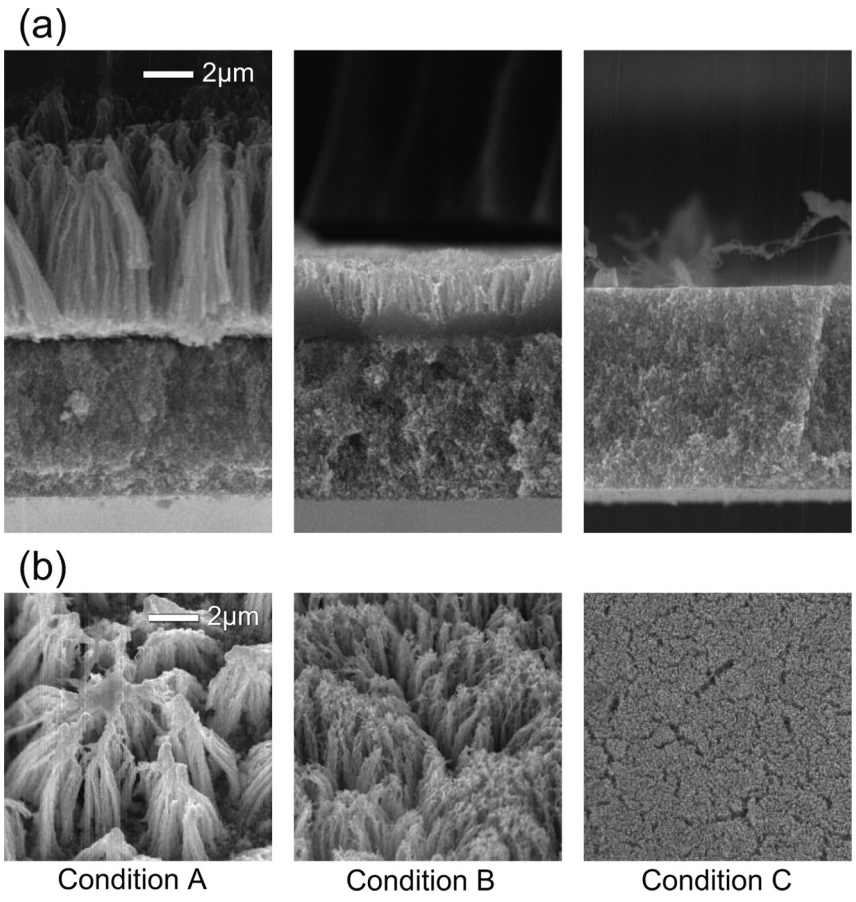


**Fig. 9.** Through-chip porous areas after the RIE process were observed by SEM. (a) Si chips were cleaved, and cross-sections were observed by setting the chips perpendicular to the microscope stage. (b) The bottoms of the opened fuel channels were observed by inclining the Si chips.

no residual layer. The maximum power density was 450 mW $cm^{-2}$, which is much larger than in our previous report, of 145 mW $cm^{-2}$. As expected, the residual porous Si layer has negative impact on the fuel cell performance. The polarization curve of the condition C exhibited a significant voltage drop around 1 A $cm^{-2}$. This was probably due to water flooding in the catalyst layer. Conventional PEFC does not generally show such a steep drop when pure oxygen is supplied to cathode. The fuel channels of our miniature fuel cell were just holes at this point, because a simple fabrication process was preferred with a small through chip porous area to maintain mechanical strength. It was supposed that accumulated water trapped and formed a water film on the channel bottoms, because

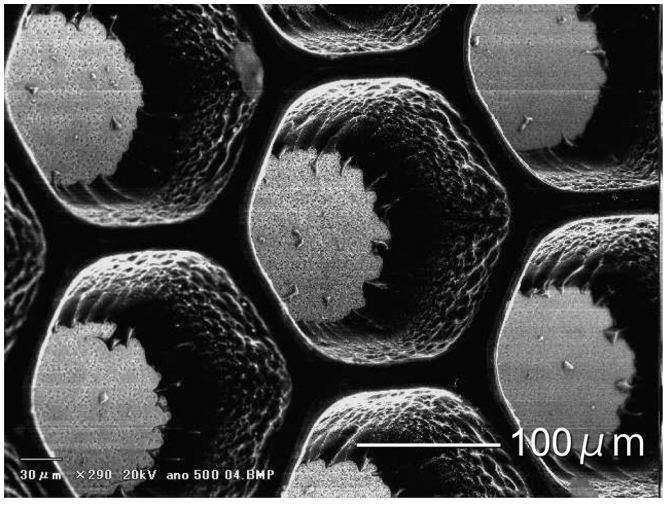


**Fig. 10.** Wide image of the monolithic Si electrode with almost no residual porous Si layer.

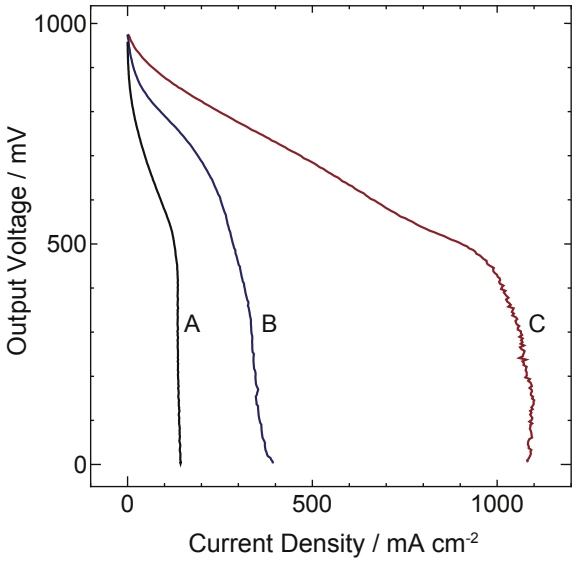


**Fig. 11.** Polarization curves of the prototypes built by the three different anodization conditions. The best results under each condition were shown.

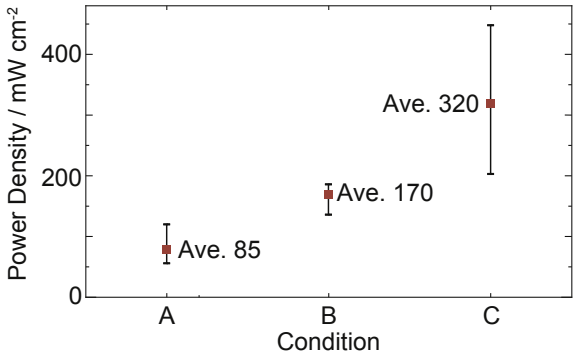


**Fig. 12.** Peak output power densities obtained of several prototypes prepared under the three conditions. Error bars show the maximum and minimum peak power.

no appropriate water drainage paths existed. Efficient channel patterns should be studied systematically.

Fig. 12 is a summary of the power generation tests. The maximum output power is shown for the three fabrication conditions. Error bars show the maximum and minimum outputs obtained by prototypes prepared under identical process conditions. Higher performance is obtained with less residual porous Si layer, but the performance still varied considerably even with no residual porous Si layer.

Several cells with smaller reaction area of $1 \times 1$ mm$^2$ were preliminarily tested for reference. Because the selected two Si wafers were used in the above experiments, those cells were produced from other Si wafers, and process condition was slightly modulated empirically from the condition C so that almost no residual porous Si layer was observed by optical microscope. Power generation tests showed large output variations from 100 to 550 mW cm$^{-2}$. It was confirmed that high power density was available by our fuel cell structure when the fabrication was carried out somehow properly, but the variation suggested that significant spatial nonuniformity in performance is inevitable in larger reaction area. These findings imply that there is a further unidentified factor in the fabrication process which is responsible for the performance instability.

## 4. Conclusion

The effect of the residual porous Si layer appearing on the channel bottom was investigated. It was found that Pt was deposited inside the residual porous Si layer, although we could not find any Pt by SEM observation. Due presumably to the Pt deposition, the residual porous Si layer has high resistivity to RIE, and further etching did not remove the residual layer. Reduction of the residual porous Si layer was attempted by adjusting the thickness of the porous Si layer in the anodization process of the crystalline Si. As the result, a catalyst layer with almost no residual porous Si layer was obtained. Prototype fuel cells were prepared under three different conditions. It was confirmed that the residual porous Si layer had a negative effect on performance, and a cell having no residual layer demonstrated a power density comparable to large scale fuel cells. Although satisfying power density was achieved, prototype cells made under the identical conditions still exhibited large variation in performance, implying that other factors as well as the residual porous Si layer influence the performance instability. Flooding of the accumulated water is proposed. A further study will be undertaken to determine the factors governing the instability, and expansion of reaction area and water drainage will also be studied.

## Acknowledgments

This work was supported partly by JSPS KAKENHI Grant Number 25390045 and the Cooperative Research Program of the "Network Joint Research Center for Materials and Devices" (MEXT Japan).

## References

[1] S.C. Kelley, G.A. Deluga, W.H. Smyrl, Electrochem. Solid-state Lett. 3 (2000) 407.
[2] S.J. Lee, A. Chang-Chien, S.W. Cha, R. O'Hayre, Y.I. Park, Y. Saito, F.B. Prinz, J. Power Sources 112 (2002) 410.
[3] T. Ito, S. Kaneko, M. Kunimatsu, Electrochem. Solid-state Lett. 12 (2009) B154.
[4] A. Kamitani, S. Morishita, H. Kotaki, S. Arscott, J. Micromech. Microeng. 18 (2008) 125019.
[5] G. D'Arrigo, C. Spinellaa, G. Arenab, S. Lorenti, Mater. Sci. Eng. C 23 (2003) 1318.
[6] M. Hayase, T. Kawase, T. Hatsuzawa, Electrochem. Solid-state Lett. 7 (2004) A231.
[7] K. Min, S. Tanaka, M. Esashi, J. Micromech. Microeng. 16 (2006) 505.
[8] N. Kuriyama, T. Kubota, D. Okamura, et al., Sens. Actuators A-Phys. 145 (2008) 354.
[9] Y. Zhang, J. Lu, H. Zhou, T. Itoh, R. Maeda, J. Microelectromech. Syst. 17 (4) (2008) 1020.
[10] Y. Zhang, J. Lu, H. Zhou, T. Itoh, R. Maeda, J. Micromech. Microeng. 19 (2009) 15003.
[11] J.P. Esquivel, T. Senn, P. Hernandez-Fernandez, J. Santander, M. Lorgen, S. Rojas, B. Lochel, C. Cane, N. Sabate, J. Power Sources 195 (2010) 8110.
[12] S. Scotti, P. Kanninen, T. Kallio, S. Franssila, J. Micromech. Microeng. 22 (2012) 094006.
[13] T. Pichonat, B. Gauthier-Manuel, J. Micromech. Microeng. 15 (2005) 179.
[14] T. Pichonat, B. Gauthier-Manuel, J. Power Sources 154 (2006) 198.
[15] S. Tominaka, S. Ohta, H. Obata, T. Momma, T. Osaka, J. Am. Chem. Soc. 130 (2008) 10456.
[16] S. Moghaddam, E. Pengwang, Y.B. Jiang, A.R. Garcia, D.J. Burnett, C.J. Brinker, R.I. Masel, M.A. Shannon, Nat. Nanotechnol. 5 (2010) 210, 1a.
[17] H. Huang, M. Nakamura, P. Su, F. Fasching, Y. Saito, F. Prinz, J. Electrochem. Soc. 154 (2007) B20.
[18] F. Iguchi, N. Sata, H. Yugami, J. Mater. Chem. 20 (2010) 6265.
[19] S. Kang, P. Heo, Y.H. Lee, J. Ha, I. Chang, S.W. Cha, Electrochem. Comm. 13 (2011) 374.
[20] S. Ji, I. Chang, Y.H. Lee, M.H. Lee, S.W. Cha, Thin Solid Films 539 (2013) 117.
[21] M. Hayase, T. Fujii, J.G.A. Brito-Neto, J. Electrochem. Soc. 158 (2011) B355.
[22] J.G.A. Brito-Neto, S. Araki, M. Hayase, J. Electrochem. Soc. 153 (2006) C741.
[23] V. Lehmann, R. Stengl, A. Luigart, Mater. Sci. Eng. B 69-70 (2000) 11.